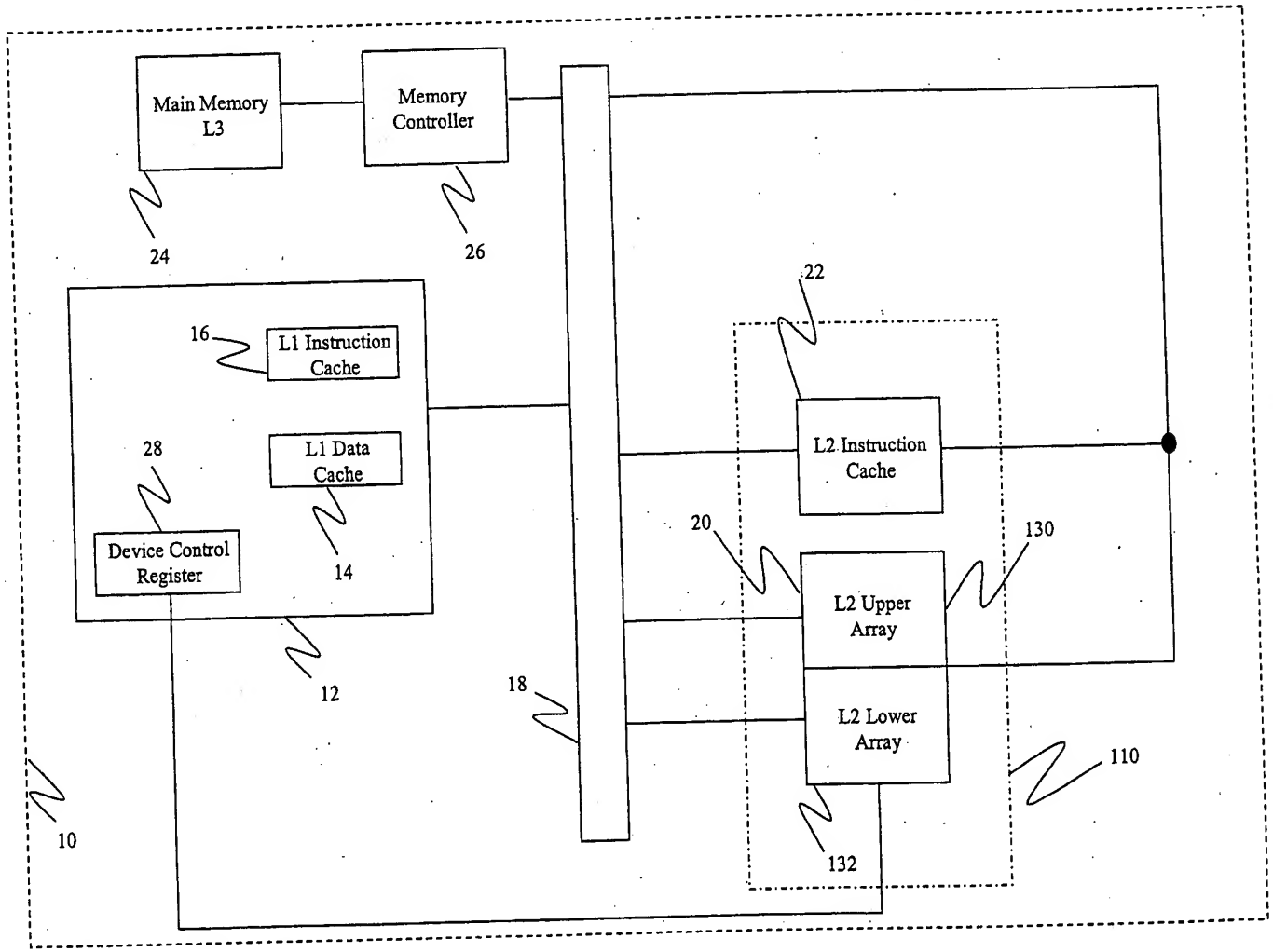

Main Memory
L3
Memory
Controller
24
26
22
16
L1 Instruction
Cache
L2 Instruction
Cache
28
L1 Data
Cache
20
130
Device Control
Register
14
L2 Upper
Array
12
18
L2 Lower
Array
110
10
132

FIGURE 1

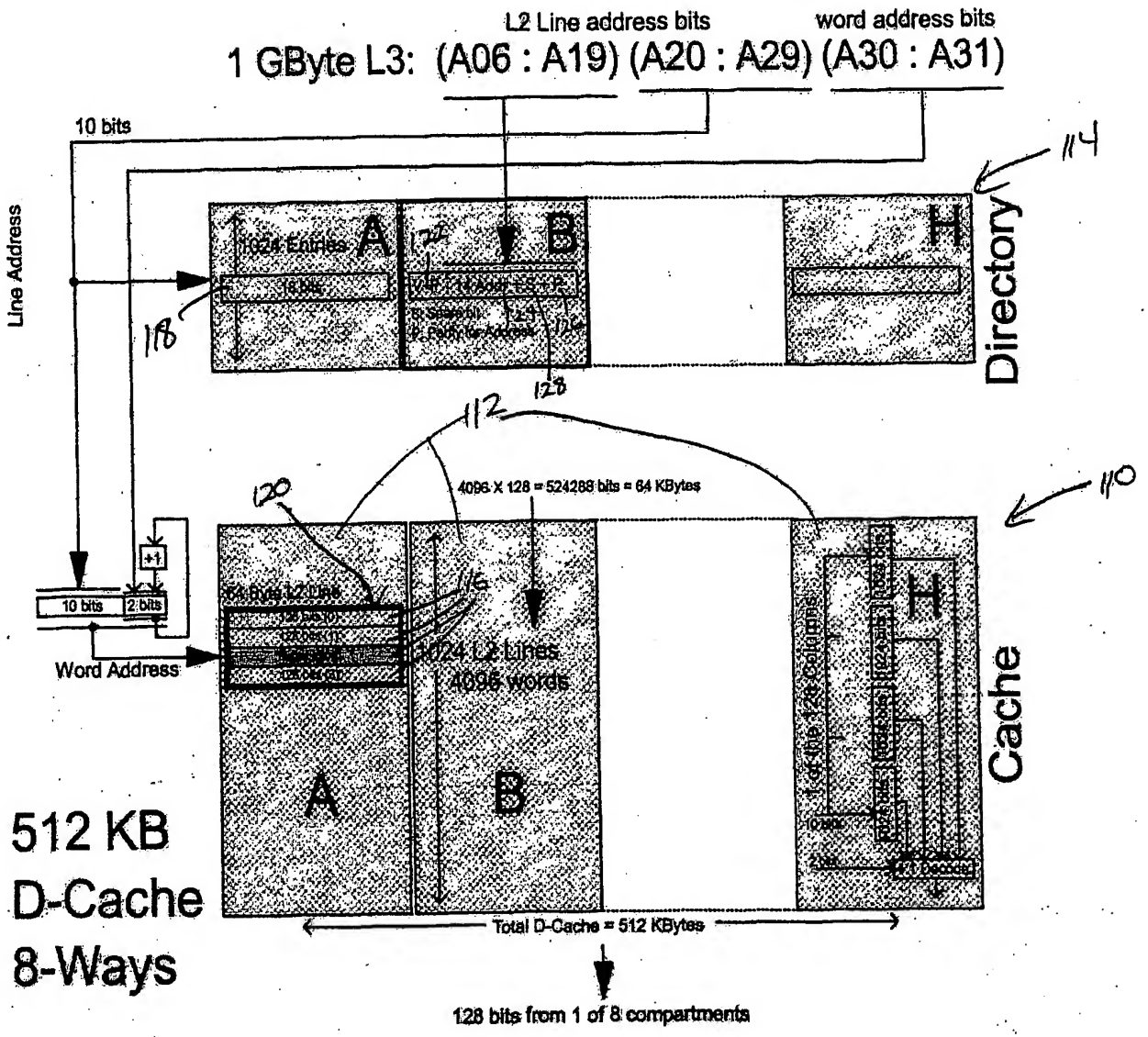
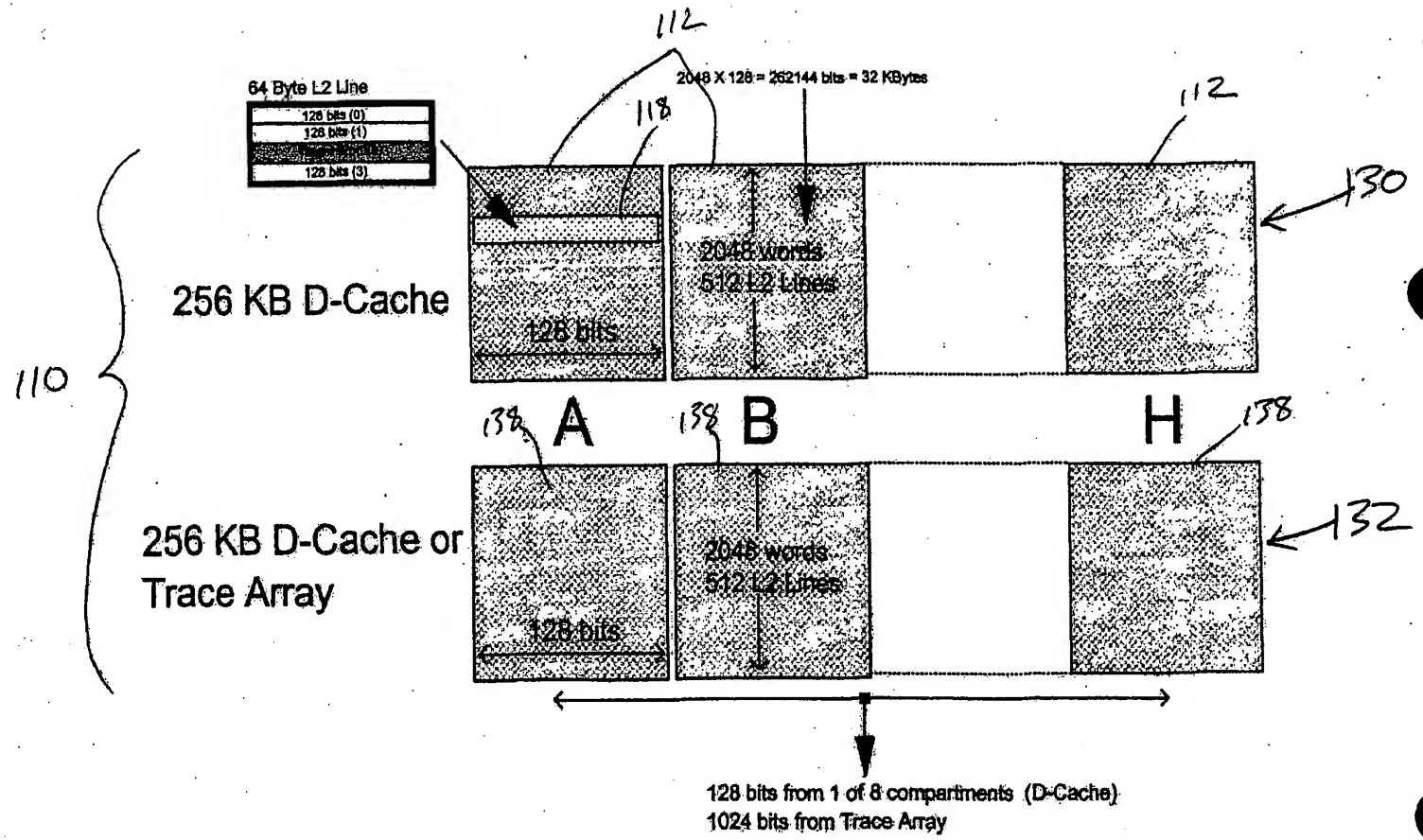
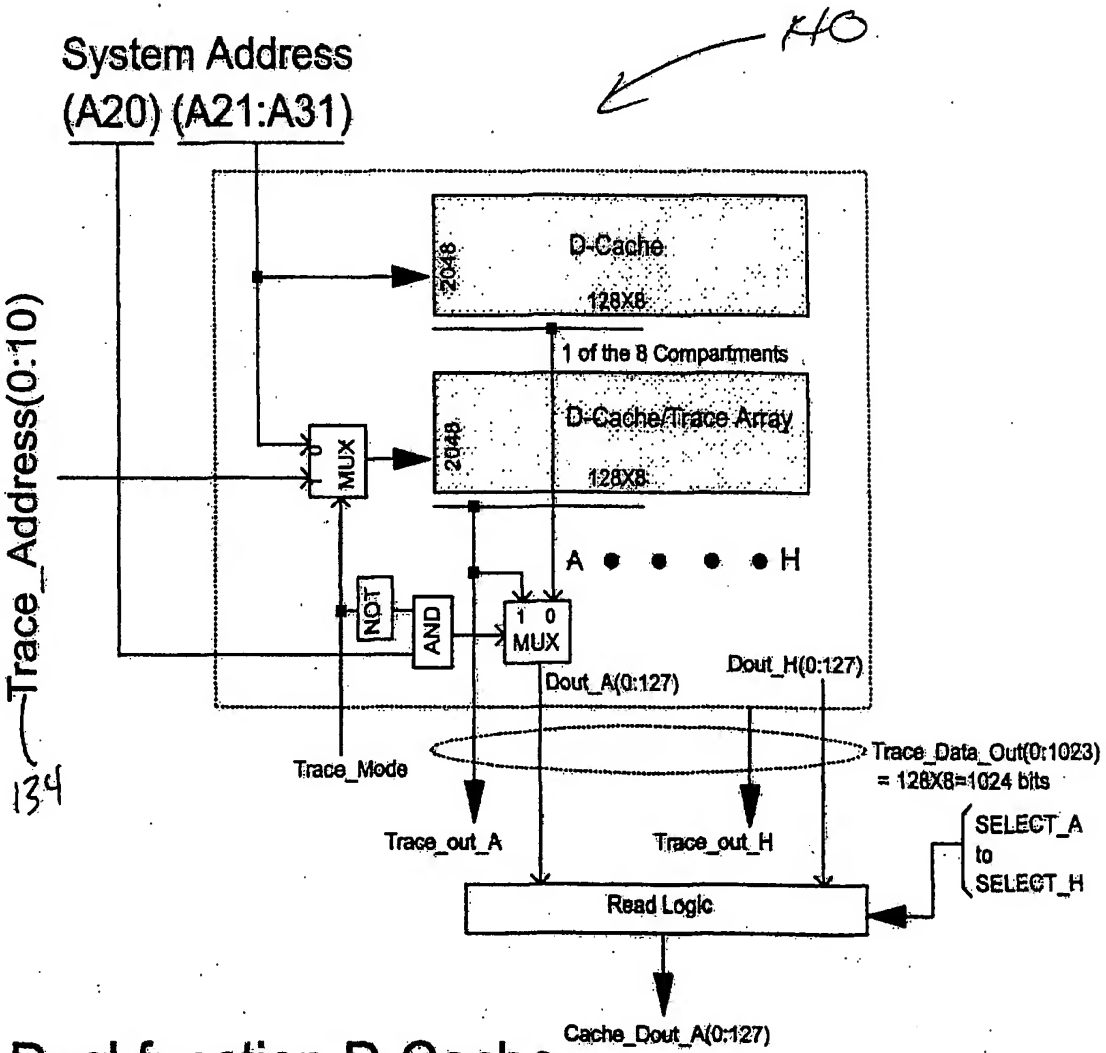

L2 Line address bits
word address bits
1 GByte L3: (A06 : A19) (A20 : A29) (A30 : A31)
10 bits
Line Address
1024 Entries
A
B
H
Directory
114
118
128
112
120
4096 X 128 = 524288 bits = 64 KBytes
110
+1
10 bits
2 bits
Word Address
1024 L2 Lines
4096 words
A
B
H
Cache
512 KB
D-Cache
8-Ways
Total D-Cache = 512 KBytes
128 bits from 1 of 8 compartments

FIG. 2



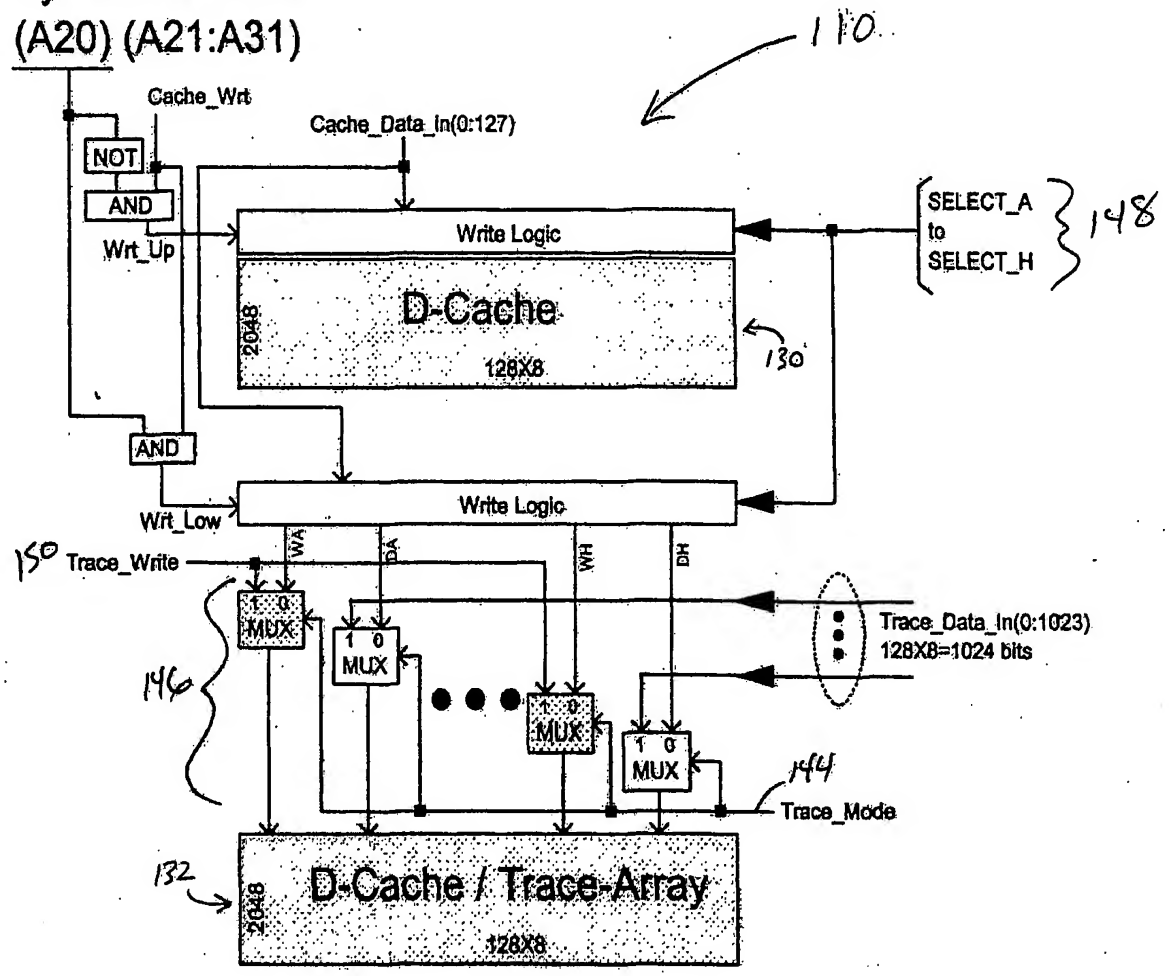
Normal Mode: 512 KB D-Cache
Trace Mode: 256 KB D-Cache and
256 KB Trace Array

FIG. 3



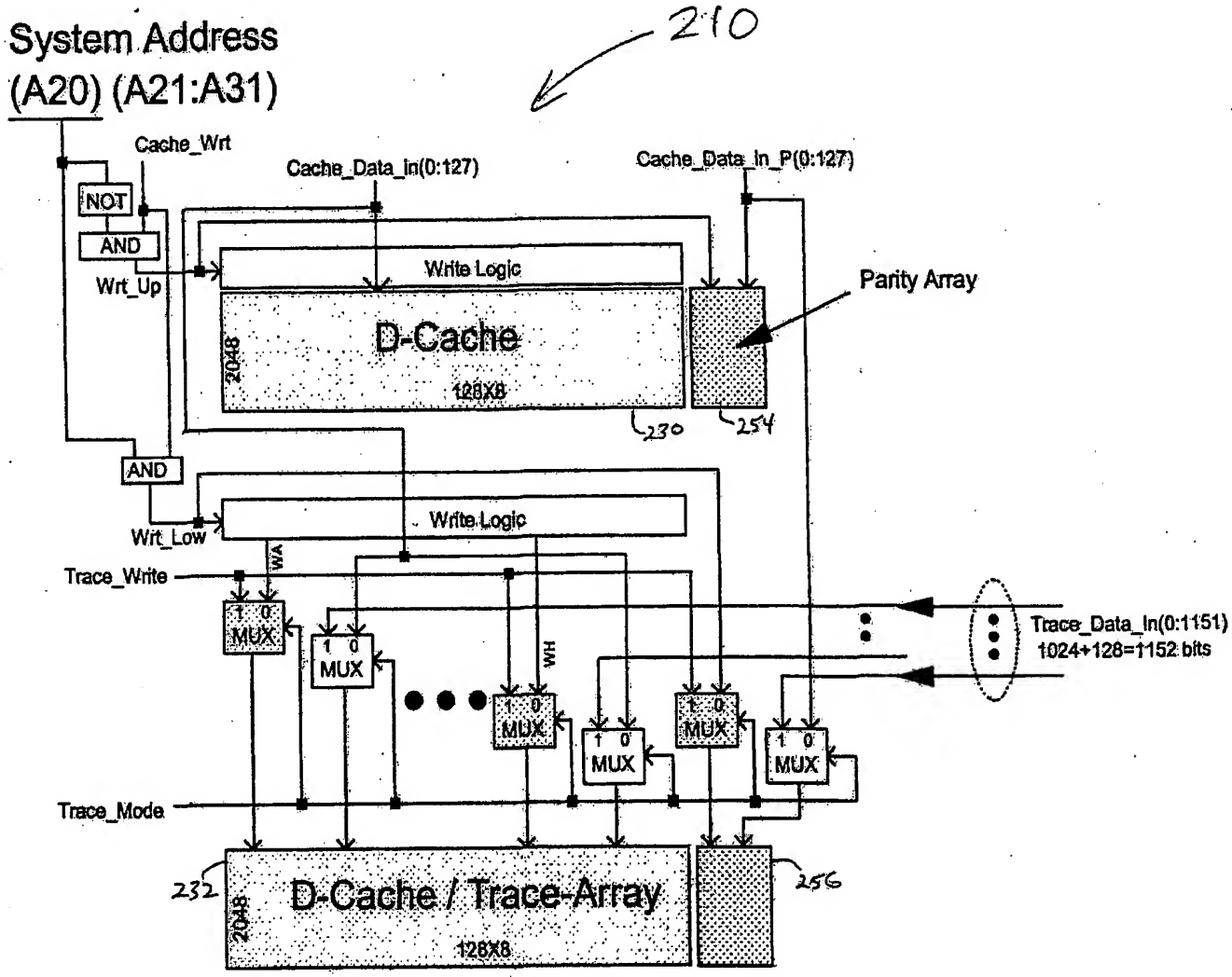
Dual function D-Cache
(Read Mode)

FIG 4



Dual function D-Cache (Write Mode). Address Control not shown (Same as Read Mode)

FIG. 5



Dual function D-Cache (Write Mode).
Parity Array as Trace.

FIG. 6

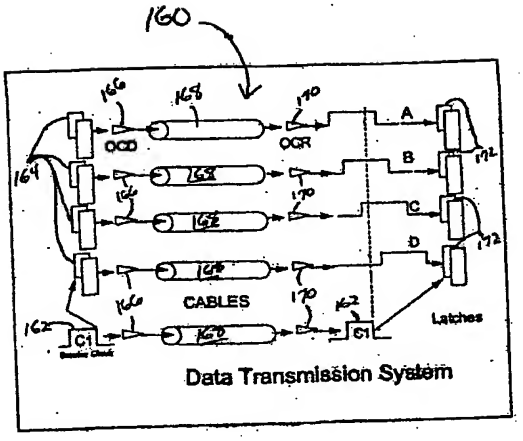


FIGURE 7

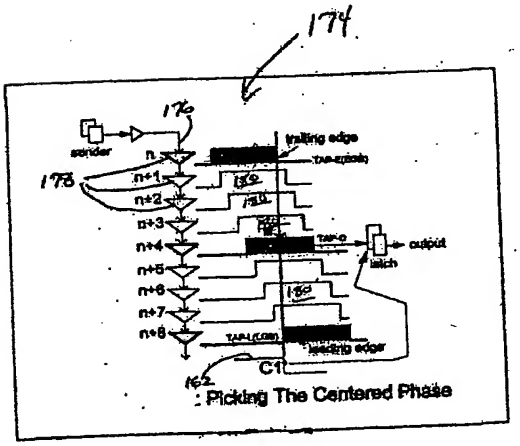


FIGURE 8

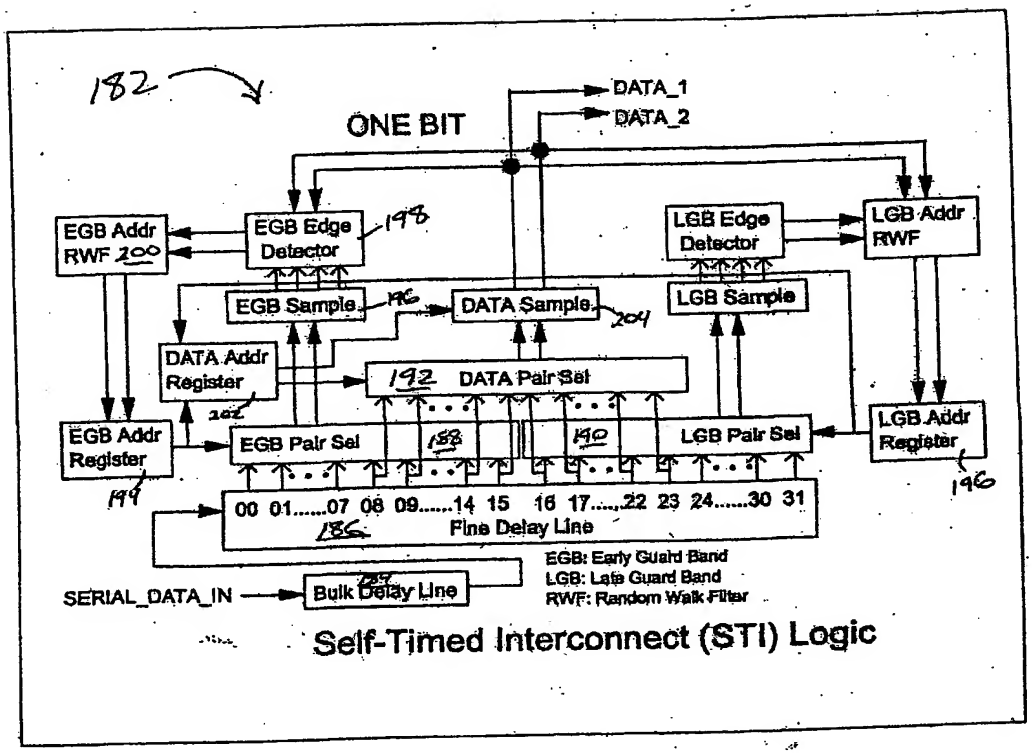

182
ONE BIT
DATA_1
DATA_2
EGB Addr RWF 200
EGB Edge Detector 198
LGB Edge Detector
LGB Addr RWF
EGB Sample 196
DATA Sample 204
LGB Sample
DATA Addr Register
192 DATA Pair Sel
EGB Addr Register 199
EGB Pair Sel 188
190
LGB Pair Sel
LGB Addr Register 146
00 01.....07 08 09.....14 15 16 17.....22 23 24.....30 31
186 Fine Delay Line
EGB: Early Guard Band
LGB: Late Guard Band
RWF: Random Walk Filter
SERIAL_DATA_IN
Bulk Delay Line
Self-Timed Interconnect (STI) Logic

FIGURE 9

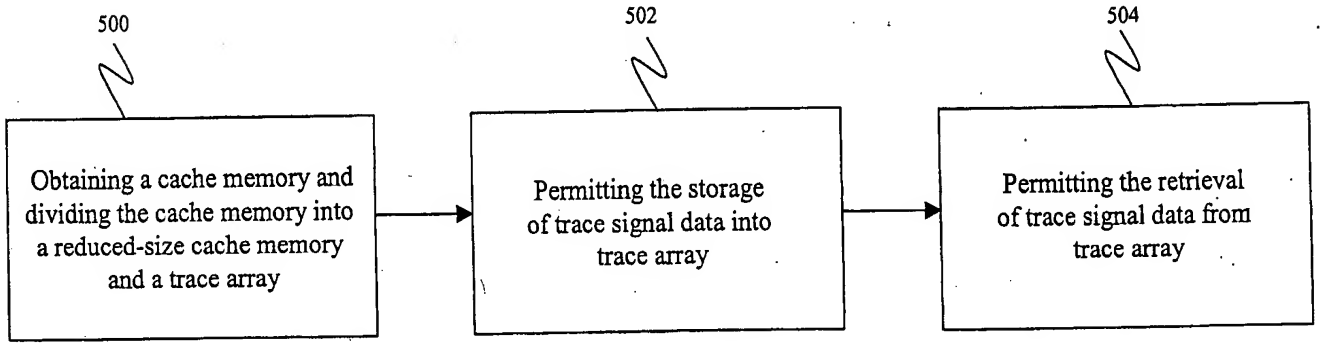

500
Obtaining a cache memory and dividing the cache memory into a reduced-size cache memory and a trace array
502
Permitting the storage of trace signal data into trace array
504
Permitting the retrieval of trace signal data from trace array

FIGURE 10